UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

ASUS COMPUTER INTERNATIONAL,

Plaintiff,

v.

ROUND ROCK RESEARCH, LLC,

Defendant.

Case No. 12-cv-02099-JST

CLAIM CONSTRUCTION ORDER

Plaintiff and Counterclaim Defendant ASUS Computer International filed this action for declaratory judgment of patent non-infringement, invalidity, and unenforceability against Defendant and Counterclaim Plaintiff Round Rock Research, LLC relating to six of Round Rock's patents: US Patent Nos. 6,570,791 ("the '791patent"); 6,765,276 ("the '276 patent"); 6,845,053 ("the '053 patent"); 6,930,949 ("the '949 patent"); 7,021,520 ("the '520 patent"); and 7,279,353 ("the '353 patent"). ECF No. 1 (April 26, 2012). Round Rock's six patents-in-suit relate to computer memory, flash memory, and digital image sensors. Round Rock counterclaimed against ASUS and Counterclaim Defendant ASUSTek Computer, Inc., (collectively, "ASUS"), alleging infringement of each of these patents. ECF No. 8 (May 18, 2012).

The Court now construes five claim terms from these patents pursuant to Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), aff'd, 517 U.S. 370 (1996), and Patent Local Rule 4–3.[1]

I. LEGAL STANDARD

The construction of terms found in patent claims is a question of law to be determined by the Court. Markman, 52 F.3d at 979. "[T]he interpretation to be given a term can only be

[1] The parties originally submitted six terms for construction, but subsequently agreed as to the meaning of one of them. The Court here construes the five remaining terms.

determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim." Phillips v. AWH Corp., 415 F.3d 1303, 1316 (Fed. Cir. 2005) (quoting Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). Consequently, courts construe claims in the manner that "most naturally aligns with the patent's description of the invention." Id.

The first step in claim construction is to look to the language of the claims themselves. "It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.'" Phillips, 415 F.3d at 1312 (quoting Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1115 (Fed. Cir. 2004)). A disputed claim term should be construed in light of its "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." Id. In some cases, the ordinary meaning of a disputed term to a person of skill in the art is readily apparent, and claim construction involves "little more than the application of the widely accepted meaning of commonly understood words." Id., at 1314. Claim construction may deviate from the ordinary and customary meaning of a disputed term only if (1) a patentee sets out a definition and acts as his own lexicographer, or (2) the patentee disavows the full scope of a claim term either in the specification or during prosecution. Thorner v. Sony Computer Entm't Am. LLC, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

Ordinary and customary meaning is not the same as a dictionary definition. "Properly viewed, the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent. Yet heavy reliance on the dictionary divorced from the intrinsic evidence risks transforming the meaning of the claim term to the artisan into the meaning of the term in the abstract, out of its particular context, which is the specification." Phillips, 415 F.3d at 1321. Typically, the specification "is the single best guide to the meaning of a disputed term." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed. Cir. 1996). It is therefore "entirely appropriate for a court, when conducting claim construction, to rely heavily on the written description for guidance as to the meaning of claims." Phillips, 415 F.3d at 1315. However,

while the specification may describe a preferred embodiment, the claims are not necessarily limited only to that embodiment. Id.

Finally, courts may consider extrinsic evidence in construing claims, such as "expert and inventor testimony, dictionaries, and learned treatises." Markman, 52 F.3d at 980. Expert testimony may be useful to "provide background on the technology at issue, to explain how an invention works, to ensure that the court's understanding of the technical aspects of the patent is consistent with that of a person of skill in the art, or to establish that a particular term in the patent or the prior art has a particular meaning in the pertinent field." Phillips, 415 F.3d at 1318. However, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." Id. If intrinsic evidence mandates the definition of a term that is at odds with extrinsic evidence, courts must defer to the definition supplied by the former. Id.

II. ANALYSIS

A. "Differential voltage from the array of non-volatile memory cells" — The '791 Patent

The '791 patent, titled "Flash Memory with DDRAM Interface," is directed at a flash, or non-volatile, memory device that can communicate at speeds as fast as dynamic random access memory does. The parties dispute the meaning of the term "differential voltage from the array of non-volatile memory cells" as it appears in claims 1 and 4 of the '791 patent. Round Rock proposes the construction: "the difference between the voltage in the array of nonvolatile memory cells and a reference voltage." ASUS proposes: "difference in voltage between two bit lines from the array of non-volatile memory cells."

Claim 1 recites:

> A flash memory comprising: an array of non-volatile memory cells; sense amplifier circuitry coupled to the array, wherein the sense amplifier circuitry detects a differential voltage from the array of non-volatile memory cells; data connections; and output circuitry to provide output data on the data connections on rising and falling edges of a clock signal.

Claim 4 uses the phrase in a substantially similar manner.

Round Rock attempts to support its construction by reference to the patent. In its opening

brief, Round Rock argues that the "specification describes one embodiment where the voltage in the array of nonvolatile memory cells is compared with a reference voltage, which is described as an improvement to the conventional technique of comparing currents." ECF No. 52 p. 17:21–23 (citing '791 Patent, at col. 5:10–12). Round Rock's reading of the patent is incorrect; the cited portion of the patent explains that the differential voltage (or current) sensing in the patent is an improvement over the conventional technique of current sensing, which uses a reference current. By comparison, the patented invention does not use a reference current.[2]

Instead, as ASUS argues, differential voltage sensing is described in the patent as comparing voltages from the array of memory cells itself: "differential digit lines are precharged to different voltage levels prior to accessing a memory cell." '791 Patent, at col. 5:17–20. According to the patent, differential voltage sensing involves precharging one line of the array of memory cells so that an active line may be compared to it. The patent states that precharging is not limited to a specific technique. Id., at 5:28–32.

ASUS' proposed construction is also consistent with the plain meaning of the claim language, which states that the "sense amplifier circuitry detects a differential voltage *from the array*" — meaning, from the array *itself*. Round Rock's construction ignores this express limitation and introduces the ambiguous term "reference voltage" instead. That construction would improperly sweep into the patent a technique that detects a differential voltage between a bit line on the array and a reference voltage not from the array.

In addition, the patent's citation to prior art and the embodiments included within the specification make clear that the patent teaches a differential voltage sensing technique limited to the comparison of voltages between two bit lines on the array of memory cells. See, e.g., id., at 2:47–56 (citing patent applications); Fig. 2 (illustrating sense amplifier coupled to bit lines for differential voltage sensing); 5:61–65 (describing Fig. 2). Nothing in the patent suggests that the

[2] "The present invention uses a data-sensing scheme that increases the speed of read operations and reduces current consumption *compared to conventional flash memory devices*. That is, *conventional flash memories use a current sensing technique that compares a current conducted by a memory cell to a reference current*. This sensing technique is slower than a DRAM differential voltage-sensing scheme." '791 Patent, at col. 5:7-12 (emphasis added).

term "from the array" of memory cells should not be read to mean what it says — that differential voltage sensing is limited to differences in voltage from the array of non-volatile memory cells. This is not "a situation where a party is attempting to import a limitation from the specification into the claims." The claims "already contain[] the . . . limitation." Curtiss-Wright Flow Control Corp. v. Velan, Inc., 438 F.3d 1374, 1379 (Fed. Cir. 2006).

Round Rock argues that the doctrine of claim differentiation requires the Court to adopt its construction, based on the difference between claim 6 and claims 1 and 4. Claim 6, an independent claim, describes a flash memory comprising (1) an array of memory cells with bit lines, (2) "sense amplifier circuitry coupled to the bit lines, wherein the sense amplifier circuitry detects a differential voltage between the bit lines," (3) "pre-charge circuitry coupled to pre-charge the bit lines . . . to provide an initial differential voltage," and other components. Round Rock argues that the doctrine of claim differentiation requires that the phrase "differential voltage between the bit lines" in claim 6 mean something different than the disputed phrase "differential voltage from the array of non-volatile memory cells" in claims 1 and 4.

"In the most specific sense, 'claim differentiation' refers to the presumption that an independent claim should not be construed as requiring a limitation added by a dependent claim." Id. at 1380. Though "[d]ifferent claims with different words can . . . define different subject matter within the ambit of the invention," it is also the case that "two claims with different terminology can define the exact same subject matter." Id. When applying claim differentiation "[b]eyond the independent/dependent claim scenario," the Federal Circuit has provided two principles of construction: first, "claim differentiation takes on relevance in the context of a claim construction that would render additional, or different, language in another independent claim superfluous;" second, claim differentiation "cannot broaden claims beyond their correct scope." Id. (citation omitted). See also Arlington Indus., Inc. v. Bridgeport Fittings, Inc., 632 F.3d 1246, 1258 (Fed. Cir. 2011) ("[C]laim differentiation should not enlarge claims beyond what the specification tells us the inventors contemplated as their invention.").

Both of these rules counsel against Round Rock's construction. First, ASUS' claim construction does not render the different language in claim 6 superfluous; the phrases "from the

array of non-volatile memory cells," in claims 1 and 4, and "between two bit lines," in claim 6, both retain their meaning if the Court adopts ASUS' construction. Second, it is Round Rock's construction that seeks to broaden claims 1 and 4 beyond their scope based on claim differentiation by rendering the phrase "from the array of non-volatile memory cells" superfluous.

ASUS' construction also captures the plain meaning of the disputed term. As described, differential voltage sensing is simply the comparison of two voltages, both of which are sensed from bit lines in the array of non-volatile memory cells. By sensing the difference in voltage between two lines on the array, the flash memory device can read data faster and at lower power cost than the conventional "reference current" sensing technique. See '791 Patent, at col. 5:14–16 ("to read numerous columns of memory cells simultaneously, conventional current sensing techniques consume a relatively large current").

The Court construes the term "differential voltage from the array of non-volatile memory cells" as it is used in claims 1 and 4in the '791 patent as "the difference in voltage between two bit lines from the array of non-volatile memory cells."

B. "Adjustable current consumption being set to the low power mode in response to a state of the mode control bit" — The '053 Patent

The '053 patent, titled "Power Throughput Adjustment in Flash Memory," is directed at a memory device "that has a selectable low current consumption (i.e., low power) mode and a high data throughput mode." '053 Patent, at col. 1:40–43. Claim 1 provides: "A memory device having an adjustable current consumption, the memory device comprising: a memory array for storing data input to the memory device during a low power mode; and a data register that stores a mode control bit, the adjustable current consumption being set to the low power mode in response to a state of the mode control bit."

The parties dispute the term "adjustable current consumption being set to the low power mode in response to a state of the mode control bit," as it appears in claim 1 of the '053 patent. Round Rock proposes a plain meaning construction, or alternatively, the construction "setting the device to a mode for low current consumption." ASUS proposes: "the amount of current consumed being dependent on the chosen mode as determined by the state of a mode control bit,

where the mode chosen is one in which a reduced quantity of bits is programmed at once."

There has been a historical trade-off between memory throughput and power conservation: non-volatile memory can either deliver high throughput, with concomitantly high current consumption, or low throughput, at low current consumption. Users whose devices are line-powered care more about throughput, because power usage is less important; users of battery-powered equipment care more about low power consumption. Id., at 1:21–35. Typically, chip designers seeking to satisfy both markets will design multiple chips aimed at one or the other, but not both. The '053 patent seeks to resolve the "need in the art for a way to choose power consumption versus throughput in a flash memory device." Id., at 1:35–37.

The invention encompasses memory devices with "a plurality of modes" that allow users, or chip manufacturers, to choose among modes of operation based on their speed and power needs. The patent describes numerous ways in which to implement the invention. In Figures 2 and 3, the "state of the mode control bit" varies the quantity of bits being programmed "in order to vary the current consumption of the memory device." Id., at 3:20–25. If the state of the mode control bit is set to a higher power mode, the maximum quantity of bits is programmed simultaneously; if it is set to the lower power mode, a reduced quantity of bits is programmed. Id., at 3:25–33. Other embodiments, however, might use the mode control bit to increase the "time between programming pulses such that data throughput is reduced," thereby decreasing current consumption. Id., at 5:4–8. In some applications, the state of the mode control bit may permanently determine the power mode the device will use; in others, it may be selectable. Id., at 3:8–12. Finally, the invention is not limited to a single bit; more than one bit may be used to select from more than two power modes. Id., at 3:5–7.

ASUS' construction is improper because it describes one embodiment to the exclusion of others. ASUS argues the definition must include the phrase "where the mode chosen is one in which a reduced quantity of bits is programmed at once." But as noted above, varying the quantity of bits programmed at once is only one embodiment encompassed by the patent; it also describes a mode control bit varying the time between programming pulses, which reduces data throughput and power consumption as well. ASUS' limiting construction of the claim does not

accord with the patent. See Phillips, 415 F.3d at 1323 ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments.").

Round Rock's construction proposes to replace the phrase "adjustable current consumption being set to the low power mode" while keeping the latter half of the disputed phrase as-is. Round Rock's construction thus reads: "setting the device to a mode for low current consumption in response to a state of the mode control bit." ASUS objects to this construction because it equates "low power mode" with lower current consumption without limitation. According to ASUS, Round Rock's construction broadens the scope of the claim to any device where a mode control bit sets flash memory in a low power mode by reducing current consumption. The Court agrees. Where ASUS' construction impermissibly excludes methods of reducing power consumption described in the patent, Round Rock's impermissibly includes methods of reducing power consumption that are unrelated to the patent.

The patent specification itself explains that the "low power mode" corresponds to a mode in which the "data throughput" of the memory device is reduced. See, e.g., '053 Patent, at Title ("Power Throughput Adjustment in Flash Memory"), Abstract ("In the low power consumption mode the mode control bit reduces the rate at which data bits are programmed . . ."), col. 1:30–32 ("Line powered devices would benefit more from programming throughput than low power consumption."), 1:40–43 (contrasting "high data throughput mode" and "low power mode"), 3:25–27 ("lower power, low throughput mode"), 3:31–33 ("Alternate embodiments use other methods to adjust the current consumption/data throughput in response to the mode control bit."), 5:41–43 ("In summary, a non-volatile memory bit is used to adjust the data throughput and, therefore, the power consumption of a memory device."). Round Rock's construction is divorced from this context.

The Court therefore construes the term "adjustable current consumption being set to the low power mode in response to a state of the mode control bit" by using the terms of the patent itself, which have a common and ordinary meaning to people of ordinary skill in the art. The Court adopts the following construction of the disputed term as it is used in claim 1 of the '053

patent: "setting the device to a low current consumption, low data throughput mode in response to a state of the mode control bit."

C. "Active Standby Mode" — The '949 Patent

The '949 patent, titled "Power Savings in Active Standby Mode," is directed to "[a]n apparatus and method for reducing the power consumed by a memory device selectively activates a power saving mode in which operation of a delay compensation circuit may be suspended during an active power down mode of operation." '949 Patent, at Abstract. The parties dispute the meaning of the term "active standby mode" with respect to its use in claims 5, 6, 7, and 20. Round Rock proposes the construction: "the mode when CKE is high and there is at least one row active in any memory bank." ASUS proposes: "mode where a delay compensation circuit is suspended in active power down mode."

The '949 patent applies to random access memories (RAM) "that utilize one or more delay compensation circuits, such as, for example, one or more delay locked loops (DLLs)." Id., at col. 1:19–20. In synchronous memory, data transfer is referenced directly to an external "clock." As data transfer speeds increase, data cannot be launched during the period of time during which the data lines are certain to be in the correct logic state. A delay compensation circuit compensates for varying conditions to ensure that data transfer occurs within the "valid window." Id., at 1:35–43. Unfortunately, a delay compensation circuit consumes significant power, even when the memory is "in a standby mode and data is not being transferred." Id., at 1:48–50. Although stopping the delay compensation circuit would stop its power consumption, it can take as many as two hundred clock cycles to resynchronize or recalibrate the delay. The Joint Electronic Devices Engineering Council (JEDEC) standard for Dynamic RAM, to which manufacturers of RAM prefer to adhere, requires the memory to exit standby mode within only one clock cycle. The patented invention seeks to address this concern.

Claim 5 recites: "A controller for a dynamic random access memory device comprising: a mode of operation wherein a transition from an active standby mode to a normal operation mode takes place in a period of more than one clock cycle." Claims 6 and 7 are dependent claims that do not contain or modify the disputed term. Claim 20 recites: "A method of enabling the

conservation of power in a power-down mode of operation of a dynamic random access memory device, comprising: transitioning from an active standby mode to a normal operation mode takes place in a period of more than one clock cycle."

The patent specification makes clear that "standby mode" is a term that encompasses multiple forms of power-down modes, including "active power-down mode," id., at 1:52–53, and "precharge power-down mode," id., at 3:30–33. See, e.g., id., at 3:26 ("In a typical DRAM, the clock enable (CKE) signal is used to place the device in a power-down or standby state."). The distinction between precharge power-down mode and active power-down mode is that the former will occur if all memory banks are idle, whereas the latter occurs if at least one row is active in any memory bank. Regardless of which power-down mode occurs, it is typically the CKE signal registering as "LOW" that places the memory device in a "power-down or standby state." Id., at 3:28. Precharge power-down mode is notated as "IDD2P," a parameter recognized in the industry that refers to the current consumed in that mode, which is typically 3–5 mA of current; "IDD3P" refers to active-power down mode, which typically consumes 20mA of current.

To reduce the IDD3P, or active power-down mode current consumption "from the typical 20mA per device to 3–5mA," id., at 4:11–15, the patent provides for "an active standby power savings mode of operation." Id., at 4:18–21. The "active standby power savings mode of operation may be provided as an optional programmable feature so that in the default mode, the device will be backwards compatible with the JEDEC standard and achieve additional power savings in a selectable power savings mode." Id., at 4:18–23. "By providing an active standby power savings mode," programmers can provide the option of exiting "power-down mode" in more than one clock cycle, or exit power-down mode in one clock transition if compliance with the JEDEC standard is necessary. Id., at 4:23–28. The invention thus allows for increased power savings at the user's option while remaining backwards compatible with the JEDEC standard.

In short, the patent is aimed at reducing the power consumed by random access memory devices in the IDD3P active power-down mode. The solution it claims is the creation of an "active standby mode." The JEDEC standard prevents the suspension or freezing of the delay compensation circuit in standby mode because it would take more than one clock cycle to

transition back to normal operation. The invention allows for a departure from the JEDEC standard, at the user or programmer's election, in order to reduce the power consumed in active power-down mode; to accomplish the power savings, the delay compensation circuit is suspended while in "active standby mode."

Claim 5 provides for a DRAM controller with a mode of operation wherein "a transition from an active standby mode to a normal operation mode takes place in a period of more than one clock cycle." The "active standby mode" clearly refers to, as ASUS argues, the "mode where a delay compensation circuit is suspended in active power down mode."

A reading of claim 13 provides helpful context. See Phillips, 415 F.3d at 1314 (Fed. Cir. 2005) ("Because claim terms are normally used consistently throughout the patent, the usage of a term in one claim can often illuminate the meaning of the same term in other claims . . . . Differences among claims can also be a useful guide in understanding the meaning of particular claim terms."); ACTV, Inc. v. Walt Disney Co., 346 F.3d 1082, 1088 (Fed. Cir. 2003) ("[T]he context of the surrounding words of the claim also must be considered in determining the ordinary and customary meaning of those terms."). Unlike claim 5, claim 13 does not contain the phrase "active standby mode." Instead, it claims a "method of transitioning from an active power-down mode of operation . . . to a normal mode of operation, comprising: suspending operation of a [delay compensation circuit] during the active power-down mode of operation; providing more than one clock cycle to exit the power-down mode of operation." Similarly, claim 17 recites a method of conserving power in a power-down mode by providing for two "active power-down" modes: first, an active power-down mode wherein the delay compensation circuit is suspended, which permits the transition to normal operating mode to take more than one clock cycle; second, an active power-down mode that does not permit suspension of the delay compensation circuit, allowing for only one clock cycle to exit the power-down mode. The first half of claim 13 (suspending the delay compensation circuit in active power-down mode) and the first half of claim 17 (same) must refer to "active standby mode," which differs from active power-down mode in that it involves the suspension of the delay compensation circuit. The novelty claimed by the patent is "active standby mode," as well as the possibility of switching between it and a traditional

active power-down mode where the circuit is not suspended.

Round Rock's proposed construction is both too narrow and too broad. It is too narrow because it focuses on the role of the CKE signal when none of the claims are so narrow. Indeed, the patent specifically disclaims any limitation based on the embodiments it uses to illustrate the invention. See Nazomi Communications, Inc. v. ARM Holdings, PLC, 403 F.3d 1364, 1369 (Fed. Cir. 2005) (patents may cover "different subject matter than is illustrated in the specific embodiments in the specification"). Round Rock's construction is too broad because it purports to define "active standby mode" as any mode in which CKE is high and at least one row of one memory bank is active. The patent disclaims such a broad definition, which could apply to circumstances unrelated to the power-down mode. See id., Figs. 5a, 5b (illustrating high CKE *after* exit from power-down mode, when at least one row of one memory bank is active because data is being transferred). For example, Round Rock's construction could apply to normal operating mode, as Round Rock's counsel acknowledged at oral argument. That would render the phrase "transition from an active standby mode to a normal operation mode" meaningless.

Round Rock's citation to a Micron technical document submitted as part of the prosecution history (but not cited by the '949 patent) titled "Calculating Memory System Power for DDR" is unavailing. Though that document discusses "active standby current" as one "mode" of DRAM operation (Round Rock asserts "current" means "mode" in this context), it does not define the term, and it assigns it the parameter IDD3N. ECF No. 54-6 p. 3. The patent does not address the IDD3N parameter and instead explicitly focuses on IDD3P (active power-down) and IDD2P (precharge power-down). Round Rock does not supply any reason to believe that that patent relates in any way to an IDD3N parameter it does not mention. In fact, as the Micron document makes clear, the IDD2P and IDD3P parameters apply when CKE is LOW, not HIGH as would obtain under Round Rock's construction. Id.

Moreover, three of the other modes of DRAM operation discussed in the Micron document include the term "standby" as well: "precharge power-down standby current," "idle standby current," and "active power-down standby current." Round Rock offers no way of harmonizing these varying uses.

The Court therefore construes the term "active standby mode" as it appears in claims 5 through 7 and 20 of the '949 patent as "mode where a delay compensation circuit is suspended in active power down mode."

D. The '353 Patent

The '353 patent is directed to and claims "passivation planarization," a method by which the uneven, or non-uniform passivation layers of an image sensor's semiconductor wafer may be made "more uniform."

i. "Planarizing"

The parties dispute the meaning of the term "Planarizing" with respect to claims 1, 3, 5, 13–17, and 20. Round Rock proposes a plain meaning construction, or, alternatively, the definition: "processing or preparing by eliminating convex and/or concave regions." ASUS proposes the definition "uniformly flattening." As set forth below, each of these constructions is subject to legitimate criticism, and the Court will adopt a variation of one of them.

A Complementary Metal Oxide Semiconductor, or CMOS image sensor, is a device commonly used in consumer-grade digital cameras. CMOS sensors typically consist of an array of pixel cells, which are composed of layers deposited in a stack. The upper surface of each layer is contiguous with the bottom surface of the next, not unlike a sandwich. The bottom layers typically include a photodiode, insulating layers, and metallization layers, which conduct electrical signals conveying color and light information detected by the photodiode. The metallization layers are composed of metal lines spaced apart at certain intervals, leaving space for light to penetrate to the photodiode below.

On top of the stack is the lens layer, through which light enters, followed by the color filter array. The patent is directed to the layers that come between the metallization layers and the color filter array: the passivation layers. These layers separate the color filter array and the lens from the metallization layers below, ensuring that moisture from above does not penetrate below, and that harmful metal material from below does not penetrate above.

The problem the patent seeks to solve arises from the deposition process. The passivation material deposited on the semiconductor "wafer" leads to a "bread-loafing" effect "as the top

surface of the passivation material rises up and over the upper metal lines" and then falls in between them where they are spaced apart. '353 Patent at col. 1:32–34. As a result of this effect, the passivation layer leaves a "non-uniform floor for a subsequent filter array coating, which may in turn lead to stress-induced striations, poor color performance and low predictability of the overall image captured by the pixel cell array." Id., at 1:37–40.

The invention claimed by the patent "provides a more uniform upper surface for the passivation layer . . . by post-deposition surface treating." Id., at 1:62–65. The "post-deposition surface treating" allows for subsequent layers to be "formed with a more uniform thickness, decreasing the possibility of stress-induced defects and ion contamination." Id., at 2:1–2. "The desired flat upper surface can be achieved by a planarization process such as chemical mechanical polishing (CMP), spin-on-glass planarization," and other mechanical or chemical methods. Id., at 4:65–5:4.

The patent first claims:

> A method of forming a semiconductor device, said method comprising: providing a passivation layer located over a final metallization layer, wherein said passivation layer includes an oxide passivation layer; planarizing a surface of said passivation layer; stopping said planarizing before reaching said final metallization layer; forming a second layer over said passivation layer; providing a color filter array layer over said second layer; planarizing a surface of said color filter array layer; and providing a lens layer over said color filter array layer.

Id., claim 1. Claims 3 and 5 claim "The method of claim 1, wherein said planarizing step includes" chemical mechanical polishing (claim 3) and etching (claim 5). Claim 13 claims a method of "forming a pixel cell of an imaging device," which proceeds in similar fashion to claim 1. Claims 14–17 are dependent claims of claim 13, which provide examples of how the "top surface of said color filter array layer is planarized." Finally, claim 20 provides for another "method of forming a pixel cell of an imaging device" that proceeds in similar fashion to claims 1 and 13.

Round Rock's proposed construction[3] — "processing or preparing by eliminating convex

[3] Round Rock first proposes a plain meaning construction, but courts should construe terms if construction is necessary to resolve a dispute about the scope of the asserted claims. See O2

and/or concave regions" — is consistent with both the term's plain and ordinary meaning and the intrinsic record because, unlike ASUS's proposed definition, it captures all embodiments in the patent and because it does not impose any unnecessary limitations on the scope of the claims, such as the degree of uniformity required.

ASUS criticizes Round Rock's proposed construction on the grounds that it is too broad because it includes the filling in of concave regions in the definition of planarizing. However, the patent clearly describes a specific embodiment of the invention which uses spin-on-glass planarization to eliminate both concave *and* convex regions:

> In another embodiment of the invention shown in FIG. 8, a flowable material such as spin-on-glass material may be applied to the oxide passivation layer 11, then heated to form the spin-on-glass layer 12 over the oxide passivation layer 11. The spin-on-glass layer 12 is provided over the uneven surface 15 of oxide passivation layer 11 *such that the spin-on-glass material fills the "valley" regions 17 and covers the "bread-loaf" regions 16*.

Id., at 5:58–65 (emphasis added).

By contrast, ASUS proposes the construction, "uniformly flattening." Round Rock correctly notes that the term "uniformly flattening" introduces ambiguity with respect to the word "uniformly." The patent itself speaks of "uniform" in relative, not absolute terms. See, e.g., id. at 1:54–58 (referring to "a *more* uniform, flat oxide passivation layer"); id. at 1:62–65 ("[t]he present invention provides a *more* uniform upper surface for the passivation layer"). Moreover, ASUS's construction would impose a limitation on the term "planarize" that appears nowhere in the intrinsic evidence.

The Court construes the term "planarizing" as used in claims 1, 3, 5, 13 through 17, and 20 in the '353 patent as – "processing or preparing by eliminating convex and/or concave regions."

ii. "Over"

The parties dispute the term "over" as it appears in claims 1, 13, 20, and 21. Round Rock

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Micro Intern. Ltd. v. Beyond Innovation Tech. Co., Ltd., 521 F.3d 1351, 1361 (Fed. Cir. 2008) (district court erred in failing to construe term "only if" even though phrase had a common meaning because parties disagreed as to its scope). The Court also is not persuaded that the term is susceptible to a plain meaning construction.

proposes a plain meaning construction, or alternatively, that "over" means "above." ASUS proposes the construction "on top of and without intervening structures."

Claim 1, reproduced above, is a method "comprising" several steps. The first step, for example, involves "providing a passivation layer located over a final metallization layer . . . ." The next step involves planarizing the passivation layer, followed by "stopping said planarizing before reaching said final metallization layer." Next, the claim provides for "forming a second layer over said passivation layer," and so it continues, building a semiconductor "wafer" like a carefully crafted, microscopic sandwich.

The Court concludes that the term "over" does not require construction because it is a commonly used English word that has a plain and ordinary meaning that is consistent with the '353 patent claims, specification, and prosecution history. Simply put, a lay jury doesn't need to hear from a judge to know how to apply the word "over".

ASUS offers several objections to the use of the plain meaning of this term. First, ASUS argues that the term must be construed to foreclose the presence of intervening structures, because the insertion of additional layers would render the invention inoperable. ASUS fails to cite any portion of the specification, however, that describes why that result would obtain. Though the patent explains that the passivation layer is meant to prevent the passage of unwanted material from below it to above it, and liquid from above to below, it does not exclude the possibility, for example, that some other layer could go in between it and the final metallization layer, including a passivation layer of a different type.

ASUS also argues that the term "over" is susceptible to multiple ordinary meanings, and therefore the Court must look to the specification to limit it to a single meaning. Though "[p]roperly viewed, the 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent," Phillips, 415 F.3d at 1321, the ordinary meaning of a term controls unless the specification contains a special meaning of the disputed term, identifies which of multiple plausible meanings holds, or otherwise resolves an ambiguity in the term, see DSW, Inc. v. Shoe Pavilion, Inc., 537 F.3d 1342, 1347 (Fed. Cir. 2008). Any special meaning of a term that limits its ordinary or common meaning must be clearly defined in the specification. Markman, 52

F.3d at 980 (citing Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388 (Fed. Cir. 1992)). Here, there is no indication in the specification or anywhere in the patent that the term "over" has been specially defined or holds more than one meaning.

The patent also is not consistent with ASUS's proposed construction. There is no part of the specification or prosecution history that uses the word "over" in the manner ASUS seeks to define it, so as to limit the term only to embodiments without an intervening structure. The word appears in the specification over a dozen times, but always in the same manner as it appears in the claims — without limitation. The Court cannot read into the claims a limitation that is not manifest in the patent. See Thorner, 669 F.3d at 1366–67 (quoting Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1325 (Fed. Cir. 2002)) (patentees may limit claim terms only through "expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope"). In fact, the patent actually uses the term "directly over" instead of "over" in a few instances to differentiate when the patentee intended a more specific meaning than simply "over." '353 patent at 4:51–53, Fig. 3A.

The fact that the embodiments of the patent illustrate the passivation layer over the next layer without intervening layers does not change this analysis. The patent disclaims any limitation based on the embodiments. Id., at 6:41–49 ("The above description and drawings illustrate preferred embodiments which achieve the features and advantages of the present invention. It is not intended that the present invention be limited to the illustrated embodiments. . . . The planarization of an oxide passivation layer to achieve a thin uniform nitride passivation layer is generally applicable to a variety of devices."). And courts do not employ a patent's embodiments to limit claim terms that otherwise have a clear ordinary and customary meaning. Comark Comm., Inc. v. Harris Corp., 156 F.3d 1182, 1186 (Fed. Cir. 1998).

"It is the claims that define the metes and bounds of the patentee's invention. The patentee is free to choose a broad term and expect to obtain the full scope of its plain and ordinary meaning unless the patentee explicitly redefines the term or disavows its full scope." Thorner, 669 F.3d at 1367. Here, the patentee chose the broad and unrestricted term "over," and it is entitled to obtain the full scope of its plain and ordinary meaning. The Court therefore agrees with Round Rock that

the term "over" as it appears in claims 1, 13, 20, and 21 does not require construction and may be given its plain meaning.

IT IS SO ORDERED.

Dated: August 9, 2013

JON S. TIGAR
United States District Judge